Name _____
NET ID _____

EXAM 2
Professor Bolton
COSC 121

Conditions: All work must be completed individually. No outside resources other than the following resources: R= {the text, your notes, a writing utensil, the exam}; you are not permitted the internet, interaction with persons, etc.

I, _____ , understand the above statements and agree to follow these terms, and upon my honor, I swear that the answers provided are of my design and of my effort alone. I have not received nor viewed answers from any source but myself (other than resources R).

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Performance

1. (10 pts) Note that each instruction class may have a different CPI. Thus we can better measure performance (average CPI) using expected values: a weighted average of probabilities of instruction type and corresponding CPIs. Assume two computing machines, each with 3 classes of instructions with corresponding CPIs. Assume the probabilities for instruction classes A, B, and C are ½, ¼, and ¼ , respectively. (Same for both processors. Assume same ISA.) Which processor is more efficient in terms of instructions per second? (No need to simplify expressions.)

Proc	Clock Rate	CPI of Class A	CPI of Class B	CPI of Class C
P1	100 MHz	2.0	1.0	1.0
P2	200 MHz	1.0	2.0	4.0

2. (20 pts) Fill out the following MIPS pipeline diagram below. For each instruction and clock cycle, identify the corresponding stage of execution. Identify any data hazards and briefly describe each. **NOTE: Add rows and columns to the diagram or table as needed. The first instruction has been filled for you. If any specs are unclear, feel free to state your assumptions and proceed accordingly. (For practical use, smartly use each row.)**

```
LW      R4      8(R16)
ADD     R2      R5      R4
SW      R2      8(R16)
ADD     R16     R16     R8
```

Part A. Assume no data forwarding; insert stalls as needed.

Inst\cycle	1	2	3	4	5	6	7	8	9
LW	IF	ID	ALU	MEM	WB				

Hazard type	**Instructions involved**	**Brief description of hazard**

Part B. Assume full data forwarding (from ALU and MEM); insert stalls as needed.

Inst\cycle	1	2	3	4	5	6	7	8	9

Hazard type	**Instructions involved**	**Brief description of hazard**

PART C. Compute CPI for this example with and without Data Forwarding. What is the CPI performance improvement ratio?

3. (20 pts) Fill out the following MIPS pipeline diagram below. For each instruction and clock cycle, identify the corresponding stage of execution. Identify any hazards and briefly describe each. ASSUME THE BRANCH IS TAKEN THE FIRST TIME IT IS ENCOUNTERED, BUT NOT TAKEN SUBSEQUENTLY. **NOTE: Add rows and columns to the diagram or table as needed. If any specs are unclear, feel free to state your assumptions and proceed accordingly.**

```
Label:  LW    R4    8(R16)
        ADD   R2    R5     R4
        BEQ   R2    R7     Label      ; branch is taken then not
        SW    R2    8(R16)
        ADD   R16   R16    R8
```

Part A. Assume full data forwarding and a static branch prediction scheme of branch taken. Assume branch determination is made in ALU stage.

Inst\cycle	1	2	3	4	5	6	7	8	9

Hazard type	**Instructions involved**	**Brief description of hazard and solution. Note which, NOOP or Flush, is needed.**

Part B. What is CPI with Branch Prediction and Data Forwarding?

Part C. Assume no branch prediction scheme was used. Instead the compiler simply inserted NOOPs until branch determination could be made. What would be the resulting CPI?

4. (10 pts) In the cache hierarchy, there is a tradeoff between cache-memory coherency and computational overhead. Within this context, VERY concisely describe (and compare and contrast) a write-through vs. write-back protocol.

5. (20 pts) Assume two similar computing machines C1 and C2. C1 uses an L2 data cache whereas C2 does not. Compute the CPI_{total} of C1 and C2 assuming Memory access consists of 20% of all instructions on average. Assume non-memory instructions have a CPI of 1. Which is more efficient? Why?

   CPI_{total} = (1 – mem_access_percentage)* $CPI_{non\text{-}mem}$ + mem_access_percentage *CPI_{mem}
   $CPI_{mem} = CPI_{ideal} + CPI_{stall}$
   $CPI_{stall} = \sum_i missRate_i * CPIpenalty_i$

Computer	L1 hit CPI (ideal aka base)	L1 miss rate	L1 miss penalty (aka L2 access time)	L2 miss rate	L2 miss penalty (aka Main Mem penalty)
C1	2	15%	20	2%	100
C2	2	10%	n/a	n/a	100

Part A. Which is more efficient? Why?

Part B. Assume that the Cache designer has the option to add a level 3 cache to cache design C1, where the access time to L3 is 40 (cycles) and the miss rate of L3 is 1%. Would the addition of L3 improve the total CPI?

Cache

6. (10 pts) Assume address space using 8 bits with addressability of 1 byte. Assume a direct mapped cache with 4, two-word blocks. Note: Assume 1 word = 4 bytes.

   Part A. Create a list of tuples to represent the FINAL STATE of the cache. Assume an initially empty cache with the subsequent memory accesses (shown here in base 10, as **byte references**): 2, 4, 32, 36, 3, 32, 2, 34. (e.g. the tenth byte is the byte located at address 10, Mem[001010]).

Tuple format: <tag, index, data content(s)>

Part B. What was the miss rate?

7. (10 pts) Restructure the cache defined in the previous question so that it has 4-word blocks. Note: you are only restructuring; the total size (number of total bits of data used) must stay the same.

   Part A. Create a list of tuples to represent the FINAL STATE of the cache. Assume an initially empty cache with the subsequent memory accesses (shown here in base 10, as byte references): 2, 4, 32, 36, 3, 32, 2, 34.

Tuple format: <tag, index, data content(s)>

Part B. What was the miss rate?